At page 3, line 19, after "set forth", insert --in the --, and after "Fig.1b", insert --arrangement--.

(NE wrong line) At page 3, line 25, after "96", delete ",".

At page 3, line 27, after "11, delete ",".

At page 4, line 27, after "in", insert --a--.

At page 5, line 5, delete "cells" and substitute" --cell--.

At page 5, line 15, after "than", delete "a".

At page 5, line 17, delete "contact" and substitute --contacts--.

At page 5, line 18, after "that", delete "is" and substitute --it--.

At page 6, line 3, after "is", insert --a--.

At page 6, line 20, after "embodiment", insert --,--.

At page 6, line 24, after "embodiment", delete ",".

At page 6, line 35, delete "the".

At page 7, line 4, after "embodiments", insert --,--, and after "column", delete ",".

At page 7, line 9, delete ",".

At page 7, line 10, delete ",".

At page 7, line 35, delete ",".

At page 7, line 36, after "that", insert --,--.

At page 8, line 1, after "1c", insert --,--.

At page 9, line 11, after "embodiment", insert --,--.

At page 9, line 32, after "Oxidation", delete "of the".

At page 10, line 2, after "regions", delete ",".

At page 11, line 10, after "implant", insert --,--.

At page 11, line 29, after "embodiment", insert --,--.

At page 13, line 2, after "122a", delete ",".

At page 13, line 13, after "embodiment", insert --,--.

IN THE CLAIMS

Please cancel claim 23.

Please amend claims 1-3, 13, 17, 20, 30 and 31 to read as follows:

1. (Twice Amended) A non-volatile memory array, comprising:

a plurality of memory cells arranged in at least one row and at least one column, each memory cell including a drain region, a source region, a channel region disposed between the drain region and the source region, a floating gate disposed over at least the channel region, and a control gate disposed over the floating gate; and

at least one conductive member disposed along at least a portion of the row, said conductive member being associated with the row and making contact with the [sources] source regions of the memory cells of the portion of the row, said conductive member being self-aligned with the memory cells of said portion of the row.

2. (Amended) The non-volatile memory array of claim 1, wherein:

said plurality of memory cells includes a first row of memory cells and a second row of memory cells adjacent to the first row, each of the memory cells along a portion of the first row sharing a common source region with at least one memory cell of the second row; and

said conductive member is disposed along at least a portion of the first and second rows, said conductive member being associated with the first and second rows and making contact with the common [sources] source regions of the memory cells in said portion of the rows, the contact of said conductive member being self-aligned with the memory cells of said portion of the rows.

3. (Amended) The non-volatile memory array of claim 1, wherein:

said plurality of memory cells includes a plurality of row pairs, at least a portion of the memory cells in each row pair having common source regions; and

a conductive member associated with each row pair, each conductive member being disposed along said portion of its respective row pair and making contact with the common [sources] source regions thereof, the contact of each

conductive member being self-aligned with the [of the] memory cells of said portion of its respective row pair.

13. (Twice Amended) In a flash erasable EPROM, a compact array, comprising:

a first flash erasable electrically programmable read-only memory (EPROM) cell formed on a substrate, and including a first cell top, a first cell first side, and a second cell second side opposite to the first cell first side;

a first cap insulator formed over the first cell top of said first flash EPROM cell;

a first insulating sidewall formed on the first side of the first flash EPROM cell; and

a conductive member disposed on at least a portion of said first insulating sidewall and making contact with a contact portion of the substrate adjacent to the first insulating sidewall, wherein said conductive member is associated with a first row of memory cells to which the first flash EPROM cell belongs and [that said conductive member] enables the selective erasing of the memory cells of the first row during an erase operation.

17. (Twice Amended) The compact array of claim 13, including:

a second flash EPROM cell formed adjacent to the first flash EPROM cell, the second flash EPROM cell including a second cell top, a second cell first side and second cell second side, the second cell second side opposing the first cell first side across the contact portion of the substrate;

a second cap insulator formed over the second cell top of said second flash EPROM cell;

a second insulting sidewall formed on the second side of the second flash EPROM cell; and

said conductive member is disposed on at least a portion of said second insulating sidewell, wherein said conductive member is also associated with a second row of memory cells adjacent to the first row, and [that said conductive

member] enables the selective erasing of the memory cells of the first row, second row, or both first and second rows during an erase operation.

20. (Twice Amended) In a flash EPROM memory device formed on a semiconductor substrate, an array configuration, comprising:

a plurality of flash EPROM cells arranged in an array having a plurality of rows extending in a row direction; and

a plurality of source connecting members extending in the row direction, each of said source connecting members disposed over, and making contact with, [sources] source regions of memory cells of each adjacent pair of [row] rows,

[wherein] each of said source connecting members enabling the selective erasing of the memory cells of one or both of the corresponding rows during an operation.

30. (Amended) [a] A non-volatile memory array, comprising:

a plurality of memory cells arranged in at least a first row of memory cells and a second row of memory cells adjacent to the first row, each of the memory cells along a portion of the first row sharing a common source region with at least one memory cell of the second row; and

a conductive member being disposed along at least a portion of the first and second rows, said conductive member being associated with the first and second rows and making contact with the common [sources] source regions of the memory cells in said portion of the rows, the contact of said conductive member being self-aligned with the memory cells of said portion of the rows,

wherein said conductive member enables the selection of the one of the first or second rows during an erase operation.

31. (Amended) The non-volatile memory array of claim 30, wherein each of said memory cells [including] includes a drain region, a source region, a channel region disposed between the drain region and the source region, a floating gate disposed over at least the channel region, and a control gate